

Semiconductors

Takeaway from Biren Tech visit

We visited Biren Tech's management last week. Biren (6082 HK, NR) is a GPGPU designer of training-and-inference accelerators, operating a fabless model with localized supply chain. **Three key takeaways from our visit include: 1) Biren's 2nd-gen BR20X product series**, with pre-silicon design completed in 2025 and commercial launch expected in 2026; **2) a broadening customer base** across AI computing platforms, telecom operators, commercial AIDC providers, and AI / LLM companies; and **3) FY25 revenue of RMB1.03bn with 2H25 contributing ~RMB0.98bn** at GPM of 55.2% (vs. 1H25's 31.9%), tracking BR166 mass-production onset; 2025 year-end inventory of RMB948.6m (+520% YoY, +58% HoH after a +292% HoH build in 1H25), addressing accelerating customer demand and ensuring supply chain resilience.

- **Company profile: Biren designs general-purpose GPU chips and GPGPU-based intelligent computing solutions for AI training and inference.** Biren reported revenue of RMB1,035mn in FY25 (+207% YoY), attributable to volume production and shipment of the BR10X series alongside delivery of multiple thousand-card-scale intelligent computing clusters.
- **Product portfolio:** The launched BR10X portfolio comprises: 1) **BR106** (single-die, four form-factor variants 106L/M/B/C), 2) **BR166** (2.5D chiplet integrating 2x BR106 dies plus 4x DRAM, three variants 166L/M/C), and 3) **BR110** (edge-inference SKU sharing the BR10X architecture). **BR166L/M entered mass production in August 2025 and BR166C in December 2025.** 2nd-gen BR20X has completed pre-silicon design in 2025 and is currently in the process of physical design and verification for tape-out (commercial launch expected in 2026), with native FP8/FP4 support and a super-node system design "LightSphere X".
- **Read-across on China GPU localisation:** The broader industry backdrop is consistent with the direction of travel on domestic AI-compute localisation. According to Reuters citing IDC, domestic vendors collectively shipped 1.65mn AI accelerator cards in China in 2025, capturing ~41% of the ~4.0mn-unit market. NVIDIA retained market leadership with ~2.2mn cards (~55% share); AMD held a modest ~4%. **Domestic players have moved aggressively to fill the void left by tightening US export controls, while there is significant retreat for the US chipmakers ([link](#)).** We expect the localization trajectory to extend further.

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China Semiconductors Sector

Kevin ZHANG
(852) 3761 8727
kevinzhang@cmbi.com.hk

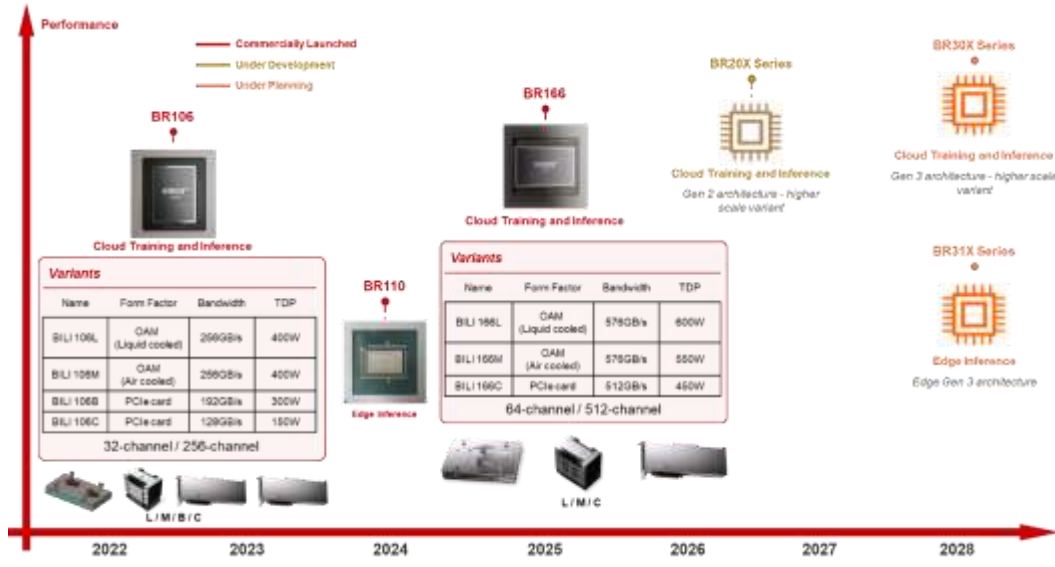
Aaron GUO
(852) 3916 3715
aaronguo@cmbi.com.hk

Company Overview

Potential 2nd-gen BR20X launch as a key catalyst

Biren completed BR20X pre-silicon design in 2025, with commercial launch expected in 2026. The 1st-Gen BR10X line was in volume shipment through late 2025, with BR20X's 2026 launch setting up the 1st-gen / 2nd-gen hand-off.

Figure 1: Biren's GPGPU product roadmap; performance ramp and variants



Source: Company data, CMBIGM

1. Architecture roadmap progression and software ecosystem depth:

- **First gen architecture:** The BR10X base architecture combines four disclosed innovations: 1) SIMT (Single Instruction Multiple Thread) for general-purpose flexibility; 2) a specialized T-core tensor engine with data recycle to reduce DRAM bandwidth pressure; 3) asynchronous data transfer with multicasting, 4) near-memory computing via NUMA/UMA/L2 Reduction.
- **Second gen architecture:** BR20X extends along four vectors: 1) native FP8/FP4 precision; 2) larger/faster memory; 3) higher interconnect bandwidth via proprietary Blink 2.0, 4) super-node scale-up, per mgmt..
- **Third gen outlook:** BR30X (cloud) and BR31X (edge) target 2028 commercial launch, and are in the process of conducting feasibility analysis and preliminary R&D, per mgmt..
- **Software stack:** BIRENSUPA native support spans PyTorch/vLLM/SGLang, extended to Triton/TileLang, with Day-0 adaptation for DeepSeek V3/R1, MiniMax M2, Zhipu GLM, Alibaba Qwen, StepFun Step, and Tencent Hunyuan, per mgmt..

Figure 2: Biren's "1+1+N+X" full stack GPGPU solution


Source: Company data, CMBIGM

Note: "1+1+N+X": "1" GPU architecture + "1" unified software platform, deriving "multiple" chips and a "comprehensive" portfolio of products.

2. Customer base broadening across AIDCs, telecom operators and LLM companies

- Biren's customer base now spans national-level AI computing platforms, telecom operators, commercial AIDC providers, AI/LLM companies, and enterprises, with AI Joint Laboratories established with leading foundation model developers and national AI platforms.
- FY25 top-five customers contributed RMB738.1m combined (~71.3% of revenue), with top customer concentration down to ~19% from ~54.5% in FY24.

3. Super-node delivery track record from 1,024-GPU to 2,048-card

Management highlighted two super-node deployments that validate capability at scale.

- The Nanjing 1,024-GPU cluster (Sep-24, RMB180m contract, 1,024 BILI 106M across 128 servers on 8-GPU BLink full-mesh UBB) delivered 95% linear scalability for large-model training.
- In 2025, Biren launched the "LightSphere X" SuperPod built on the BR10X series with ecosystem partners, using optical interconnect and distributed optical circuit switching (dOCS); a 2,048-card GPU SuperPod of this design has been deployed at a national-level computing platform. 2nd-gen BR20X extends this via a Blink 2.0 SuperPod scaling to thousand-card clusters.

4. Increase in R&D intensity; stable gross margin through scale-up

- FY25 R&D expense of RMB1,476m (+78.5% YoY) was ~143% of total revenue, reflecting sustained investment in next-generation product and technology iteration ahead of the 2nd-gen cycle. FY25 gross margin landed at 53.8%, +63bps YoY, on revenue of RMB1,034.6m (+207% YoY).

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CMB International Global Markets Limited

Address: 45/F, Champion Tower, 3 Garden Road, Hong Kong, Tel: (852) 3900 0888 Fax: (852) 3900 0800

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